A VLSI Processor Design of Real-time Data Compression for High-Resolution Imaging Radar

Wai-Chi Fang, Ph.D.

Jet Propulsion Laboratory
California Institute of Technology, Pasadena, CA 91109-8099 USA
(818) 354-4695, e-mail: wfang@blacks.jpl.nasa.gov

Abstract For the high-resolution imaging radar systems, real-time data compression of raw imaging data is required to accomplish the science requirements and satisfy the given communication and storage constraints. The Block Adaptive Quantizer (BAQ) algorithm and its associated VLSI processor design have been developed to provide a real-time data compressor for high-resolution imaging radar systems.

Introduction

Most future Earth observation platforms and a number" of planetary missions contain synthetic aperture imaging radar as a major part of their payloads for regional and large scale high resolution surface imaging [1]. The limited resources of spacecraft constrain the maximum downlink data rates and data volume available to its imaging radar payload.

To accomplish the science requirements and satisfy the resource constraints, a real-time data compressor based on block adaptive quantization algorithm and its associated VLSI processor design have been developed to provide an efficient data compression for advanced imaging radar system.

Algorithm and Simulation

The theory of block adaptive quantization is based on the fact that synthetic aperture imaging radar (SAR) data statistics are Gaussian with the variation in the power of the return echo being a slow function of range. The echo power profile is periodic with respect to pulse number and varies slowly on a burst to burst basis. Block adaptive quantization has proved to be a practical data compression method to achieve a 8:2 compression ratio for single-beam SAR raw data of the Magellan mission to Venus [2]. For advanced imaging

data compression, due to multiple-beam imaging requirements, the improved block adaptive quantizer (BAQ) encodes the SAR raw data using thresholds generated from the current burst instead of the previous burst as in the case for the single beam Magellan SAR. This current-burst BAQ scheme alleviates the performance degradation due to the multiple-beam SAR imaging requirements and reduces the hardware design, complexity by minimizing the encoding look-up table. This improved BAQ algorithm has been verified in detail with simulation results,

Architecture Design

Figure 1 shows a baseline architecture for the BAQ and its interfaces with other portions of the imaging radar system. The digital radar data sample sequence {X(t)} is converted from the analog radar data waveforms by the analog-to-digital converter (ADC) at a sampling rate of up to 30 MHz. Each digital radar data sample is an 8-bit sign-magnitude data, These radar data samples are selectively packed in 16-bit words and loaded into the science data buffer during the receive-window interval. The digital radar data samples of each echo of a burst are partitioned into blocks, where each block includes Ns successive samples, For the i-th burst, the radar data sample of the j-th echo can be denoted by $X(l + k\ \mathrm{Ns}, j)$. Here l is the sample index in a block, k is the block index in an echo, j is the echo index in a burst, $0 \le l \le \mathrm{Ns} - 1$, $0 \le k \le \mathrm{Nb} - 1$, $0 \le j \le \mathrm{Ne} - 1$, and Ns, Nb , and Ne , are positive integers. A RAM-based science data buffer is used to buffer a burst of radar data from the ADC to alleviate the real-time processing rate requirement for the adaptive threshold estimator. After a burst is loaded into the science data buffer, the BAQ reads the corresponding radar data samples for the adaptive threshold estimator to calculate the thresholds. The quantizer encodes the corresponding samples in the k-th block whenever the threshold of the k-th block, TH_k, is available. The encoding process is done by using an optimized coding look-up table. The word packer packs the encoded data from each burst into words. Then the flight computer unit collects the packed data and the thresholds into the science data memory.

VLSI Implementation

An algorithm-specific VLSI processor based on the block adaptive quantization has been developed on a

single VLSI chip using the 1-μm CMOS technology. Detailed functional design of the BAQ chip is shown in Fig. 2. The chip layout design is shown in Fig. 3. The silicon area for the BAQ chip is 6171 μm x 6629 μm. The encoding rate is up to 30 M pixels per second and the end-to-end pipeline latency equals to 32 clock cycles. The encoding rate is determined by the longest delay path of the accumulator. For Radar imaging system, a high speed data compression system can be implemented by using one BAQ chip to achieve a compression ratio of 8:1, 8:2, or 8:4 at 30 M pixels per second.

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Reference

[1] C. Elachi, Spaceborne Radar Remote Sensing: Applications and Techniques, IEEE Press, 1987,

[2] R. Kwok, W. T. K, Johnson, "Block Adaptive Quantization of Magellan SAR Data", IEEE Trans. on Geoscience and Remote Sensing, Vol. 27, No. 4, July 1989.

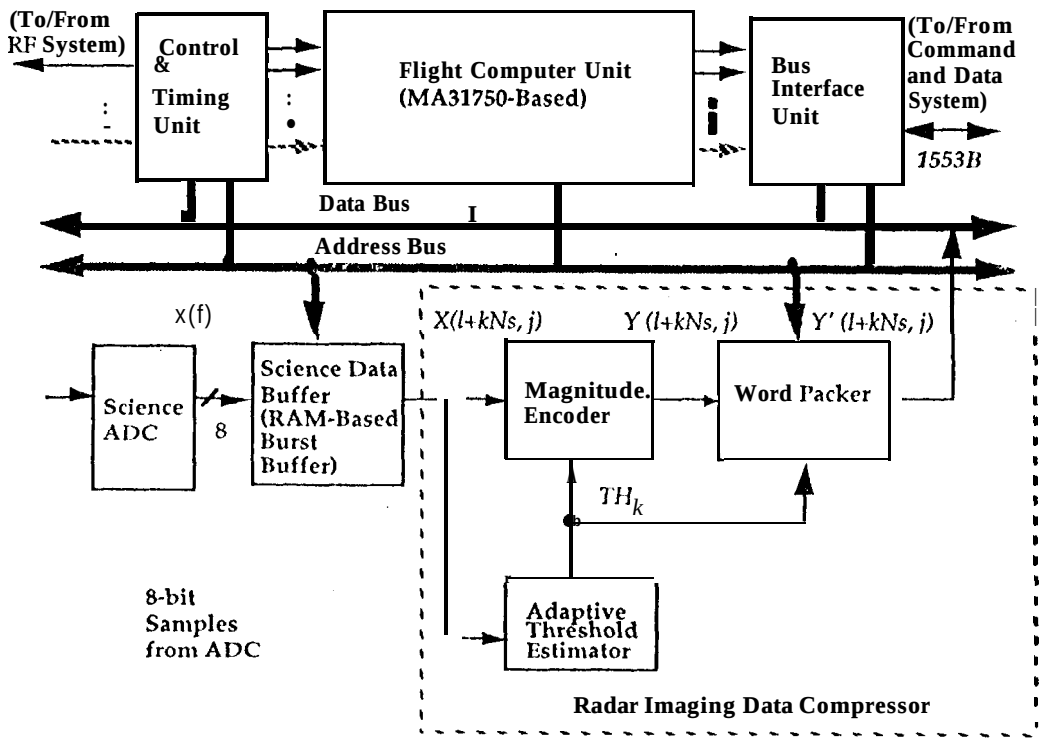

Fig. 1 Architecture design for the BAQ and its role in the imaging radar

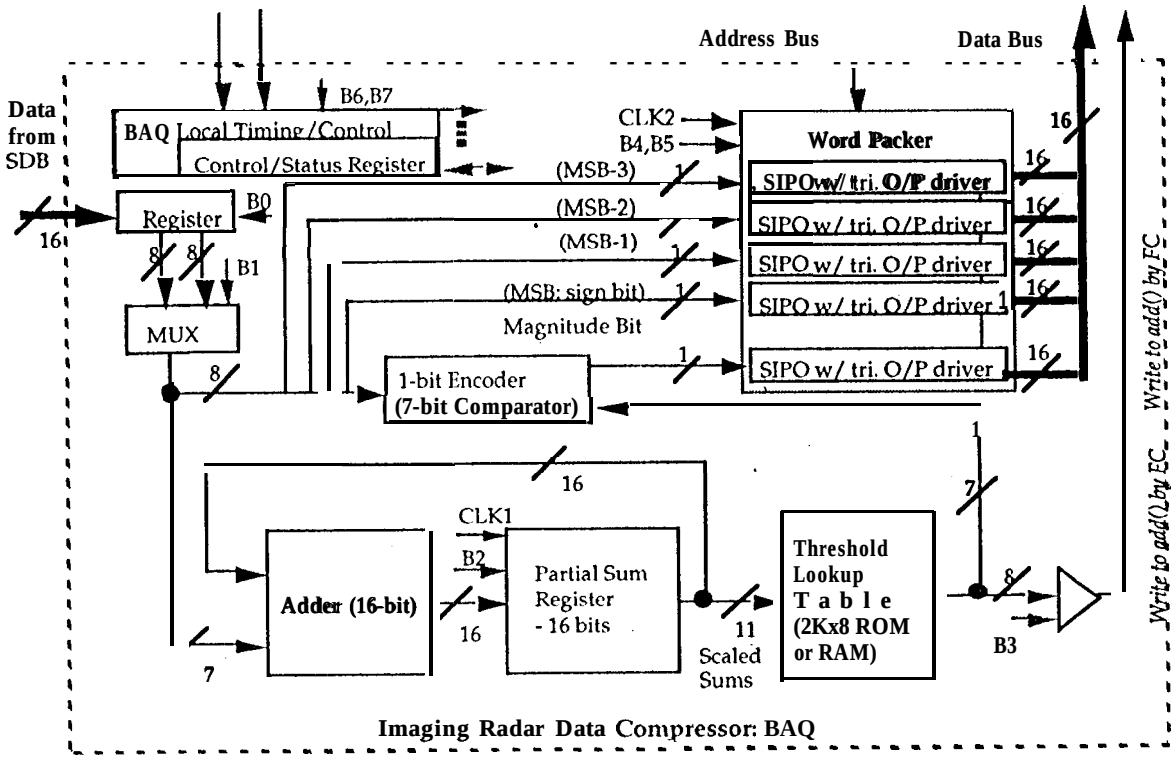

Fig. 2. Functional Design of the BAQ for imaging radar data compression.

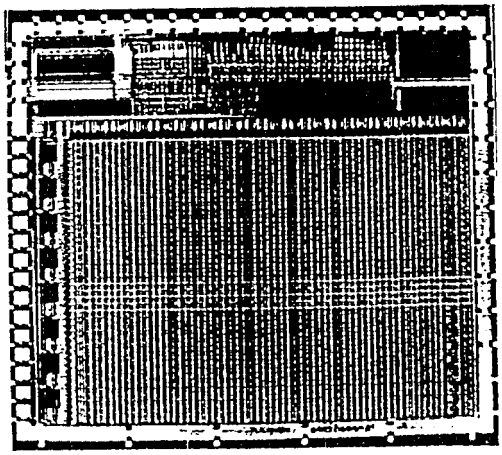

Fig. 3. VLSI Chip Layout Design of the BAQ.